



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,996	07/26/2000	R. Dean Adams	FIS9-2000-0138US1	8495

30743 7590 11/06/2002

WHITHAM, CURTIS & CHRISTOFFERSON, P.C.
11491 SUNSET HILLS ROAD
SUITE 340
RESTON, VA 20190

EXAMINER

CHAUDRY, M. MUJTABA K

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/625,996	ADAMS ET AL.
	Examiner	Art Unit
	Mujtaba K Chaudry	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on ____.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-17 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
 5) Claim(s) ____ is/are allowed.
 6) Claim(s) 1-17 is/are rejected.
 7) Claim(s) ____ is/are objected to.
 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 26 July 2000 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 11) The proposed drawing correction filed on ____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). ____.
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) Other: ____

DETAILED ACTION

Drawings

1. The drawings are objected to because:

- In all of the included drawings the font size needs to larger and clearer.
- The margins in the drawing need to be appropriated such that information is not cut off from the page(s).
- In Figure 1, “From Memory(s) Under Test” should perhaps be in a block. It is not evident which arrows (if all) are pointing to this item.
- This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

- On page 22, (Abstract) line 6 the terms “including them” should be eliminated.
- On page 2, line 2 the term “have” should be “has” and on line 32 the term “toether” should perhaps be “together.”
- On page 3, line 16 the term “and” should be deleted.

- On page 3, line 31 and page 14, line 32 the term “further” should perhaps be replaced with “furthermore.”
- On page 4, line 10 the term “where” should perhaps be replaced with “when.”
- On page 10, lines 13-14 the close parenthesis is missing “)”.
- On page 10, the applicant implies that Figures 1-3 are not admitted as prior art since they are used to convey the present invention. Applicant is reminded that a Figure should be designated by a legend such as --Prior Art—if it is of prior art. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
- On page 11, line 10 the terms “is begun” should perhaps be replaced with “begin.” Also on line 20 a grammatical error exists.
- On page 12, line 29 the reference number 160 should perhaps be replaced with 165 according to Figure 2.
- Throughout the specification the all the reference numbers should be in parenthesis (e.g. page 12 lines 11, 12 etc)
- The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Schwarz (USPN 5982681).

As per claims 1 and 8, Schwarz teaches (title, Figure 2 and claim 1) a method and apparatus for a reconfigurable built-in self-test circuit, which is on an integrated circuit with embedded memory. Schwarz clearly teaches all the limitations in Figure 2, as stated in the present application. Furthermore, Schwarz (claim 1) teaches an embedded memory within the integrated circuit that is configured to store input data (analogous to external test instructions in the present application) from the external tester. A built-in self-test circuit is included and generates BIST data patterns (analogous to the default test instructions in the present application).

As per claims 2-3, 7, 9-10 and 16, Schwarz teaches (col. 3, lines 13-21) the integrated circuit to include an embedded device, a BIST circuitry and a comparator. Schwarz further points out that the embedded device may be a memory, a multiplier or some other digital circuit module (analogous to the initialization storage means in the present application). The examiner would like to point out that the default test instructions (in the present application) are analogous to the address and data signals (col. 3, line 19) of Schwarz.

As per claims 4 and 11, Schwarz teaches (col. 5, lines 13-19) the BIST data patterns (analogous default test instructions in the present application) are provided (activated) when a debug signal is de-asserted.

As per claims 5-6 and 12-15, Schwarz teaches (col. 3 lines 58-65) a means for controlling the test operation by means of a external debug signal that is part of the system and is analogous to control signal in the present application. When the debug signal is de-asserted (analogous to activating means) the data patterns (analogous to default test instructions in the present applications) are routed to the embedded memory.

As per claim 17, Schwarz teaches (col. 3 -- col. 4, lines 41-54) a method for performing system level tests including a integrating circuit having BIST circuitry wherein manufacturing level and board level testing are performed. The board level testing has already been shown above. As for the manufacturing level testing, Schwarz teaches (col. 4 lines 40-55) an integrated circuit in a socket controlled by the test equipment. Furthermore, Schwarz teaches this system to monitor the BIST process and compile a summary of the results when the test is complete.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Schwarz teaches a method and apparatus for a reconfigurable built-in self-test circuit, which is on an integrated circuit with embedded memory. Schwarz clearly anticipates all the limitations stated in the present application. Applicant is further invited to visit additional prior art included in this action.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.



Mujtaba Chaudry

Art Unit 2133

October 31, 2002



ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100